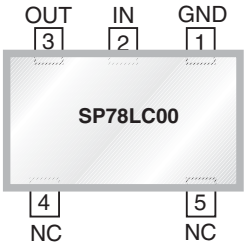
SP78LC00

Micropower, 100mA CMOS LDO Regulator

FEATURES

- Low Dropout Voltage, 160mV @ 100mA
- High Output Voltage Accuracy, 2%
- Guaranteed 100mA Output
- Ultra Low Shutdown Current, 1μA Max
- Ultra Low GND Current
  - 110μA @ 100mA Load
  - 28μA @ 100μA Load
- Fast Transient Response
- 78dB PSRR @ 100Hz
- 40dB PSRR @ 400kHz
- Extremely Tight Load and Line Regulation
- Very Low Temperature Coefficient
- Current and Thermal Limiting
- Unconditionally stable with 1μF Ceramic
- 5 Pin SOT-23 Package
- Fixed 3.0V Output
- 100mA Replacement for 50mA MC78LC



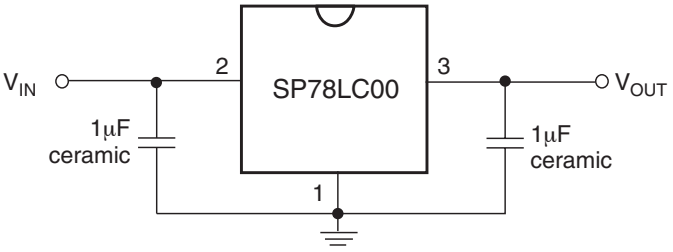
APPLICATIONS

- Mobile Phone Data Cables
- Laptop, Notebook and Palmtop Computers
- Battery-Powered Equipment
- Consumer/ Personal Electronics
- SMPS Post-Regulator
- DC-to-DC Modules
- Medical Devices
- Data Cable
- Pagers

DESCRIPTION

The SP78LC00 is a CMOS LDO designed to meet a broad range of applications that require accuracy, speed and ease of use. This LDO offers extremely low quiescent current which only increases slightly under load, thus providing advantages in ground current performance over bipolar LDOs. The LDO handles an extremely wide load range and guarantees stability with a 1μF ceramic output capacitor. It has excellent low frequency PSRR, not found in other CMOS LDOs and thus offer exceptional Line Regulation. High frequency PSRR is better than 40dB up to 400kHz. Load Regulation is excellent and temperature stability is comparable to bipolar LDOs.

The SP78LC00 is available in fixed 3.0V output voltage version in a small SOT-23-5 package.



Typical Application Diagram

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ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (V_{IN}) ..... -2V to 7V
Output Voltage (V_{OUT}) ..... -0.6 to (V_{IN} +1V)
Enable Input Voltage (V_{EN}). ..... -2V to 7V
Power Dissipation (P_D) ..... Internally Limited, **Note 3**
Lead Temperature (soldering 5s). ..... 260°C
Storage Temperature ..... -65˚C to +150˚C

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

OPERATING RATINGS

Input Voltage (V_{IN}) ..... +2.5V to +6V
Enable Input Voltage (V_{EN}) ..... 0V to +6V

Junction Temperature (T_J) ..... -40˚C to +125˚C
Thermal Resistance, SOT-23-5 (θ_{JA}) ..... **Note 3**

ELECTRICAL SPECIFICATIONS

$V_{IN} = V_{OUT}$ +1V, I_L = 100µA, C_{IN} = 1.0µF, C_{OUT} = 1.0µF, T_J = 25°C , **bold** values indicate -40°C ≤ T_J ≤ 125°C unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Accuracy, (V_{OUT})	Variation from specified V_{OUT}	-2 **-3**		2 **3**	% %
Output Voltage Temperature Coefficient, **Note 4**, ($\Delta V_{OUT}/\Delta T$)			60		ppm/°C
Line Regulation, ($\Delta V_{OUT}/ V_{OUT}$)	V_{IN} = (V_{OUT} + 1V) to 6V		0.03	**0.2**	%/V
Load Regulation, **Note 5**, ($\Delta V_{OUT}/ V_{OUT}$)	I_L = 0.1mA to 100mA,		0.07	**0.25**	%
Dropout Voltage, **Note 6**, ($V_{IN} – V_{OUT}$)	I_L = 100µA		0.2	4 **7**	mV mV
	I_L = 50mA		70	120 **160**	mV mV
	I_L = 100mA		160	250 **300**	mV mV
Ground Pin Current, **Note 7**, (I_{GND})	I_L = 100µA		28	45 **50**	µA µA
	I_L = 50mA		60	120 **150**	 µA
	I_L = 100mA		110	200 **250**	µA µA
Power Supply Rejection Ratio, (PSRR)	Frequency = 100Hz, I_L = 10mA Frequency = 400kHz, I_L = 10mA		78 40		dB dB
Current Limit, (I_{CL})	V_{OUT} = 0V	**100**	150	**200**	mA
Thermal Limit	Regulator Turns Off Regulator Turns On		162 147		°C °C
Thermal Regulation, **Note 8**, ($\Delta V_{OUT}/\Delta P_D$)			0.05		%/W

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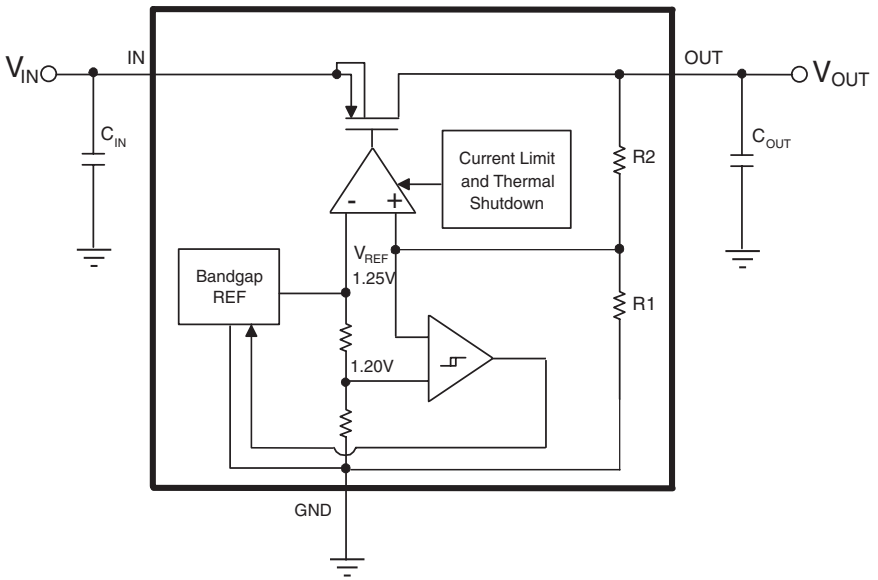
$V_{IN} = V_{OUT} + 1V$, $I_L = 100\mu A$, $C_{IN} = 1.0\mu F$, $C_{OUT} = 1.0\mu F$, $T_J = 25°C$, **bold** values indicate $-40°C \le T_J \le 125°C$ unless otherwise noted.

Note 1. Exceeding the absolute maximum rating may damage the device.
Note 2. The device is not guaranteed to function outside its operating rating.
Note 3. The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{D\ (MAX)} = (T_{J\ (MAX)} - T_A) / q_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The q_{JA} of the SP78LC00 (all versions) is 220°C/W mounted on a PC board with minimum copper area (see "Thermal Considerations" section for further details).
Note 4. Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
Note 5. Load Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range; from 0.1mA to 100mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.
Note 6. Dropout Voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.
Note 7. Ground pin current is the regulator quiescent current. The total current drawn from the supply is the sum of the load current plus the ground pin current.
Note 8. Thermal regulation is defined as the change in output voltage at a time "t" after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 100mA load pulse at $V_{IN} = 6V$ for t = 10ms.

PIN ASSIGNMENTS

PIN NUMBER	NAME	FUNCTION
1	GND	Ground
2	IN	Supply Input Voltage
3	OUT	Regulator Output Voltage
4,5	NC	No Connection

FUNCTIONAL DIAGRAM



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General Overview

The SP78LC00 is a CMOS LDO designed to meet a broad range of applications that require accuracy, speed and ease of use. This LDO offers extremely low quiescent current which only increases slightly under load, thus providing advantages in ground current performance over bipolar LDOs. The LDO handles an extremely wide load range and guarantee stability with a 1μF ceramic output capacitor. It has excellent low frequency PSRR, not found in other CMOS LDOs and thus offer exceptional Line Regulation. High frequency PSRR is better than 40dB up to 400kHz. Load Regulation is excellent and temperature stability is comparable to bipolar LDOs. Thus, overall system accuracy is maintained under all DC and AC conditions. Current Limit and Thermal protection is provided internally and is well controlled.

Architecture

The SP78LC00 has a current limit of 150mA. The LDO has a two stage amplifier which handles an extremely wide load range (10μA to 100mA) and guarantees stability with a 1μF ceramic load capacitor. The LDO amplifier has excellent gain and thus touts PSRR performance not found in other CMOS LDOs. The amplifier guarantees no overshoot on power up. The amplifier also contains an active pull down, so that when the load is removed quickly the output voltage transient is minimal; thus output deviation due to load transient is small and fairly well matched when connecting and disconnecting the load.

An accurate 1.250V bandgap reference is bootstrapped to the output. This increases both the low frequency and high frequency PSRR. Unlike many LDOs, the bandgap reference is not brought out for filtering by the user. This tradeoff was maid to maintain good PSRR at high frequency (PSRR can be degraded in a system due to switching noise coupling into this pin). Also, often leakages of the bypass capacitor or other components cause an error on this high impedance bandgap node. Thus, this tradeoff has been made with "ease of use" in mind.

Protection

Current limit behavior is very well controlled, providing less than 10% variation in the current limit threshold over the entire temperature range of the SP78LC00. The SP78LC00 has a current limit of 150mA. Thermal shutdown activates at 162°C and deactivates at 147°C. Thermal shutdown is very repeatable with only a 2 to 3 degree variation from device to device. Thermal shutdown changes by only 1 to 2 degrees with Vin change from 4V to 7V.

Input Capacitor

A small capacitor, 1μF or higher, is required from V_{IN} to GND to create a high frequency bypass for the LDO amplifier. Any ceramic or tantalum capacitor may be used at the input. Capacitor ESR (effective series resistance) should be smaller than 3Ω.

Output Capacitor

An output capacitor is required between V_{OUT} and GND to prevent oscillation. A capacitance as low as 0.22μF can fulfill stability requirements in most applications. A 1μF capacitor will ensure unconditional stability from no load to full load over the entire input voltage, output voltage and temperature range. Larger capacitor values improve the regulator's transient response. The output capacitor value may be increased without limit. The output capacitor should have an ESR (effective series resistance) below 5Ω and a resonant frequency above 1MHz.

No Load Stability

The SP78LC00 will remain stable and in regulation with no external load (other than the internal voltage driver) unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications.

Thermal Considerations

The SP78LC00 is designed to provide 100mA of continuous current. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. To determine the maximum power dissipa-

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tion in the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

$$P_D = \frac{(T_{J(max)} - T_A)}{\theta_{JA}}$$

$T_{J(max)}$ is the maximum junction temperature of the die and is 125°C. T_A is the ambient operating. θ_{JA} is the junction-to-ambient thermal resistance for the regulator and is layout dependent.

The actual power dissipation of the regulator circuit can be determined using one simple equation:

$$P_D = (V_{IN} - V_{OUT})*I_{OUT} + V_{IN}*I_{GND}$$
$$\cong (V_{IN} - V_{OUT}) * I_{OUT}$$

Substituting $P_{D(max)}$ for P_D and solving for the operating conditions that are critical to the application will give the maximum operating conditions for the regulator circuit. For example, if we are operating the SP78LC00-3.0V at room temperature, with a minimum footprint layout, we can determine the maximum input voltage for a set output current.

$$P_{D(max)} = \frac{(125°C - 25°C)}{(220°C/W)} = 454mW$$

To prevent the device from entering thermal shutdown, maximum power dissipation can not be exceeded. Using the output voltage of 3.0V and an output current of 100 mA, the maximum input voltage can be determined. Ground pin current can be taken from the electrical spec's- table (I_{GND}=110µA at I_{OUT}=100mA). The maximum input voltage is determined as follows:

$454mW = (V_{IN} – 3.0V)*100mA + V_{IN}*0.11mA$

Solving for V_{IN}, we get:

$$V_{IN} = \frac{(454mW + 300mW)}{100.11mA}$$

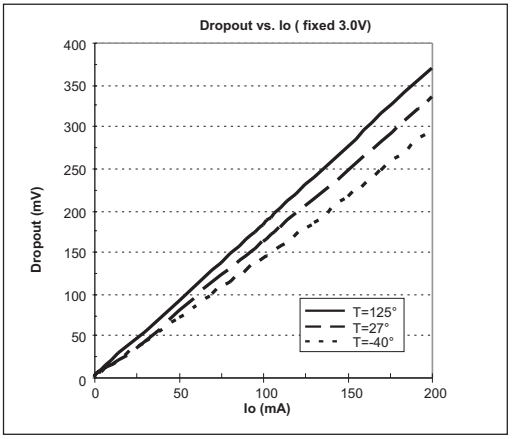
After calculations, we find that the maximum input voltage of a 3.0V application at 100mA of output current in an SOT-23-5 package is7.53V.

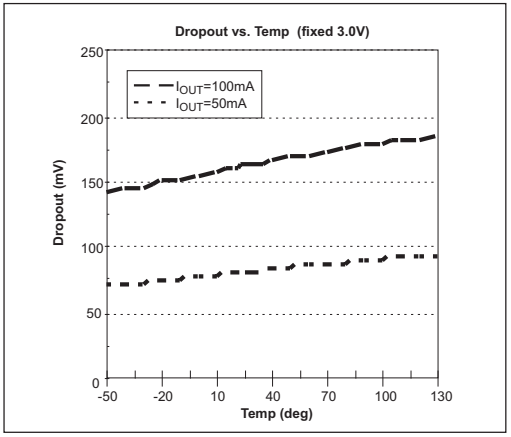
Dual-Supply Operation

When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

TYPICAL CHARACTERISTICS

27°C, V_{IN} = 5.5V, I_O = 0.1mA, C_{IN} = C_{OUT} = 1µF unless otherwise specified.





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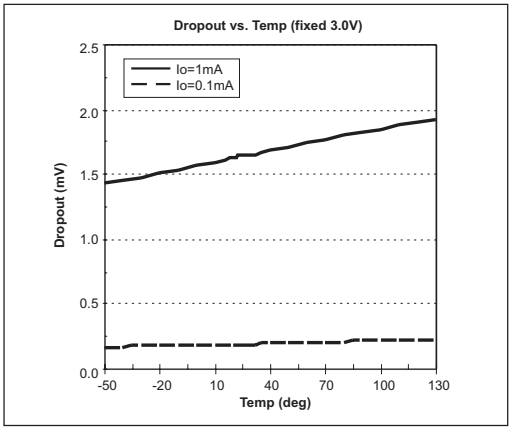

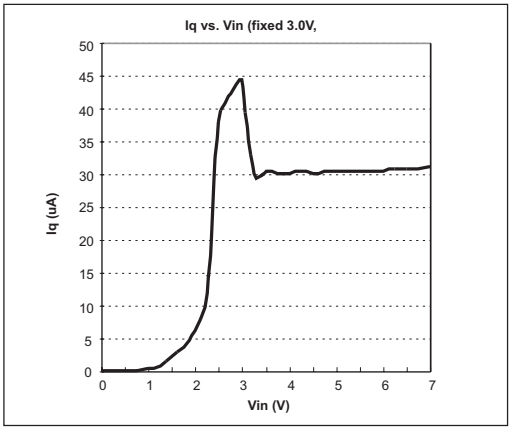

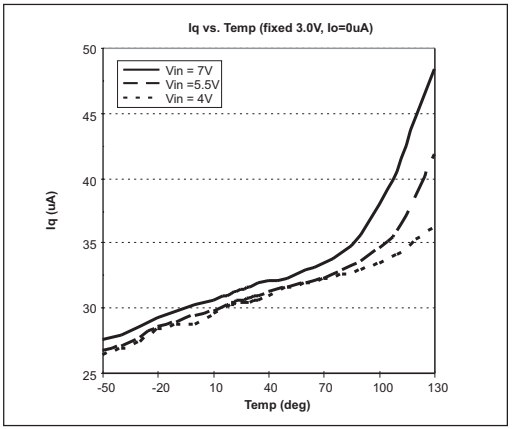

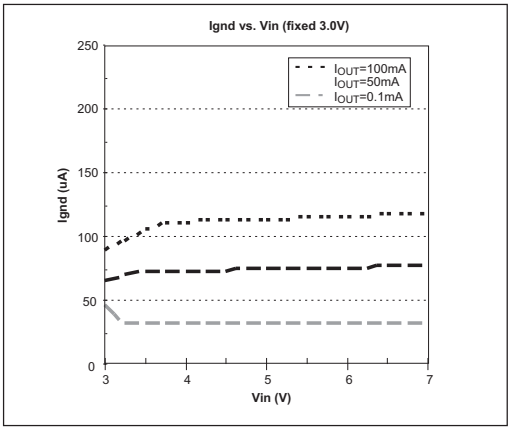

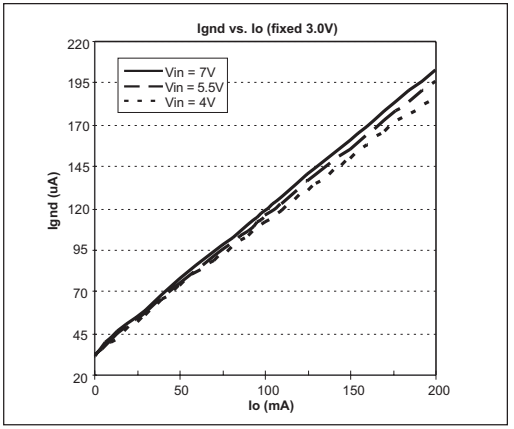

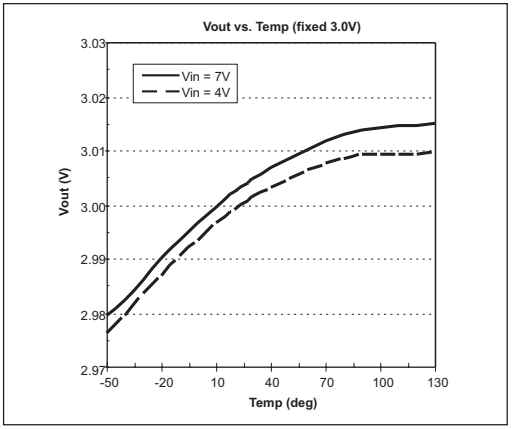

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TYPICAL CHARACTERISTICS: Continued

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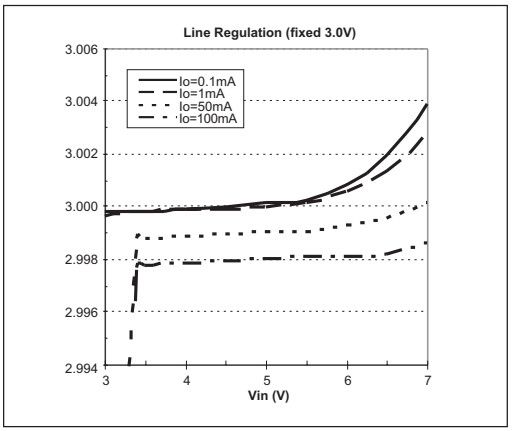

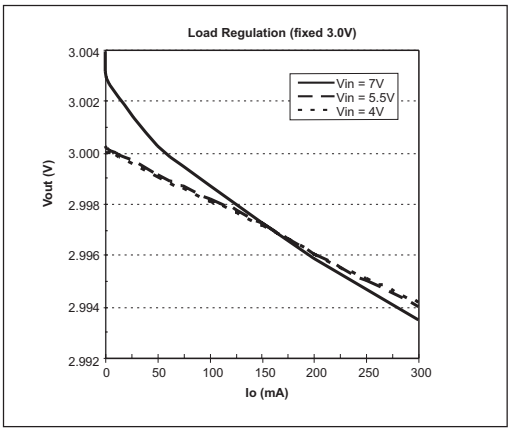

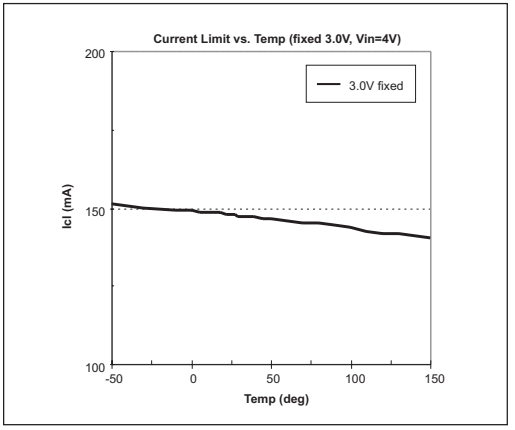

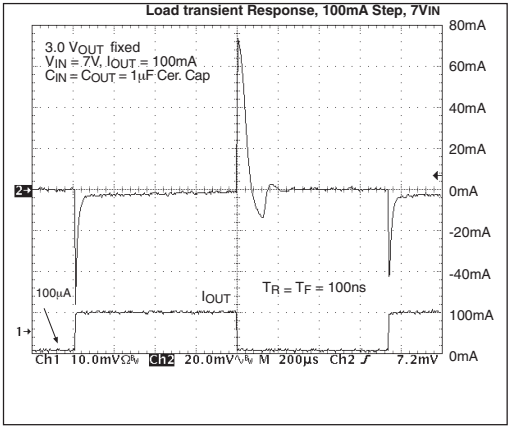

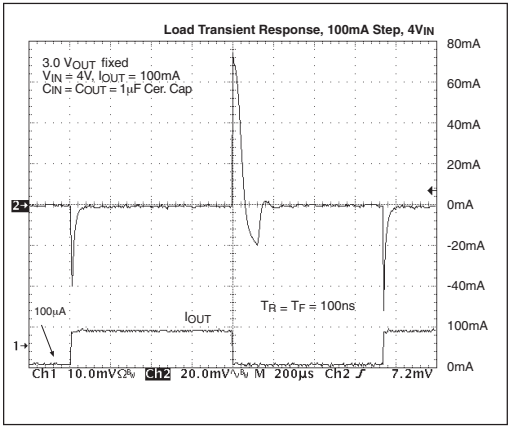

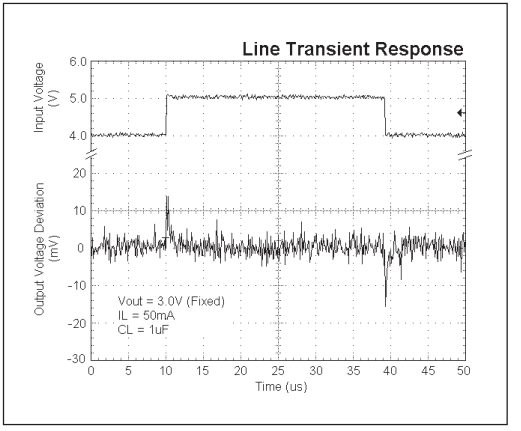

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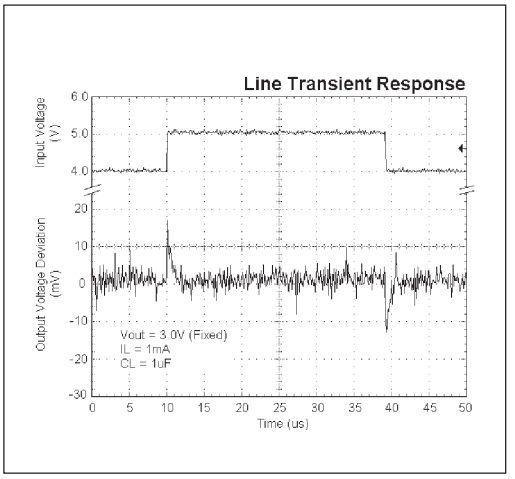

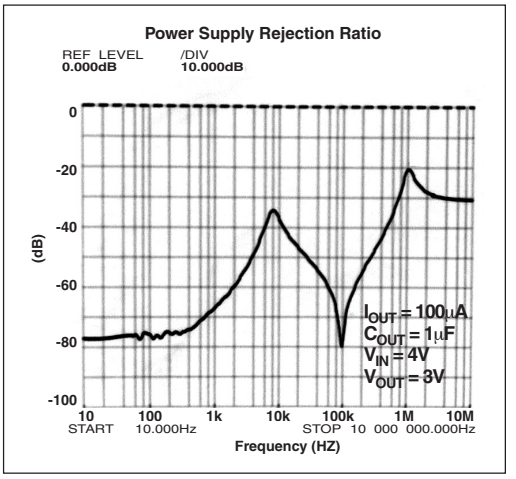

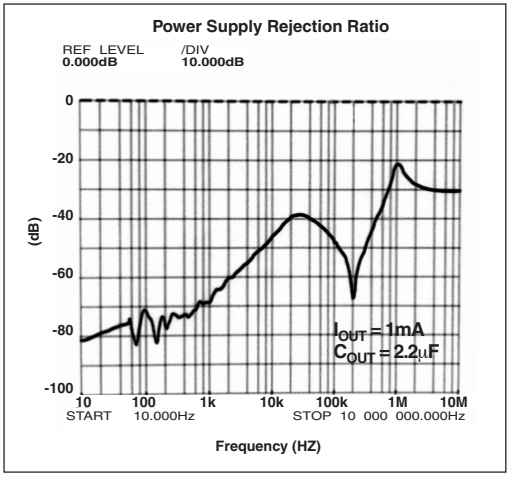

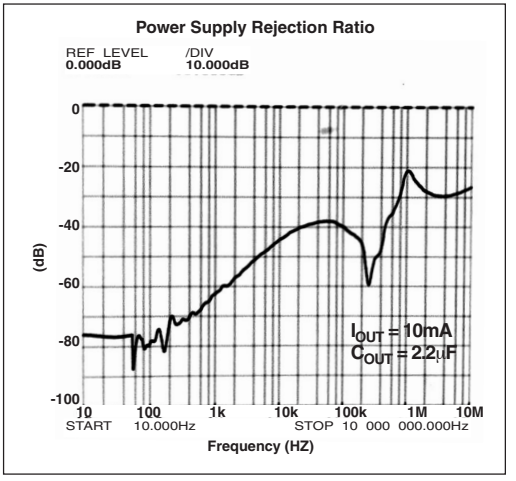

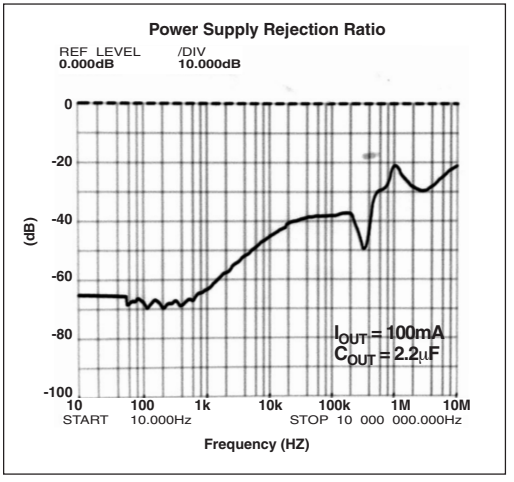

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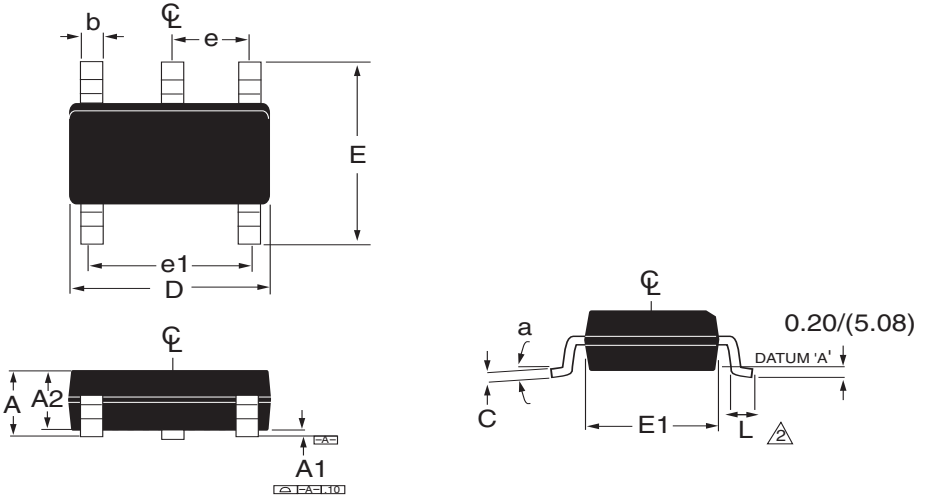

SYMBOL	MIN inch / mm	MAX inch / mm
A	0.90 / (22.86)	1.45 / (36.83)
A1	0.00 / (0.00)	0.15 / (3.81)
A2	0.90 / (22.86)	1.30 / (33.02)
b	0.25 / (6.35)	0.50 / (12.7)
C	0.09 / (2.286)	0.20 / (5.08)
D	2.80 / (71.12)	3.10 / (78.74)
E	2.60 / (66.04)	3.00 / (76.2)
E1	1.50 / (38.1)	1.75 / (38.1)
L	0.35 / (8.89)	0.55
e	0.95ref / (24.13)	
e1	1.90ref / (48.26)	
a	0°	10°

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ORDERING INFORMATION

Part Number	Topmark	Temperature Range	Package Type
SP78LC30EM5	T1	-40˚C to +125˚C	SOT-23-5
SP78LC30EM5/TR	T1	-40˚C to +125˚C *(Tape & Reel)*	SOT-23-5

SIGNAL PROCESSING EXCELLENCE

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